REMARKS

This Amendment is responsive to the Office Action mailed on August 23, 2006. Claims 1-20 are amended. New claims 23-26 are new. Claims 1-26 are pending.

Claims 1-22 are rejected as being indefinite. The claims are amended herein to overcome the indefiniteness rejection. Withdrawal of this rejection is respectfully requested.

Claims 1-3, 5-10, and 12-22 are rejected under 35 U.S.C. § 102(b) as being anticipated by Peters (US 4,606,025).

Claim 4 and 11 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Peters.

Applicants respectfully traverse these rejections in view of the amended claims and the following comments.

Discussion of Amended Claims

Claims 1-20 are amended to overcome the Examiner's rejections under 35 U.S.C. § 112. Claims 1-20 are also amended for clarity and to place the claims into better form for U.S. examination.

In addition, claim 1 is amended to specify a control method for mixed-signal ICs.

New claims 23 and 24 correspond to original claims 21 and 22, respectively, and depend from claim 7.

New claims 25 and 26 correspond to original claims 21 and 22, respectively, and depend from claim 14.

Discussion of Peters

Claims 1-3, 5-10, and 12-22 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Peters. This rejection is respectfully traversed. An anticipation rejection requires that each and every element of the claimed invention as set forth in the claim be provided in the cited reference. See *Akamai Technologies Inc. v. Cable & Wireless Internet Services Inc.*, 68 USPQ2d 1186 (CA FC 2003), and cases cited therein. As discussed in detail below, Peters does not meet

the requirements for an anticipation rejection.

Peters discloses a system for automatically testing a plurality of memory arrays on selected memory array testers. The disclosure of Peters is limited to memory ICs, and does not disclose or remotely suggest testing methods for mixed signal ICs. Those skilled in the art will appreciate that memory ICs are the simplest and the easiest type of ICs to test. Other types of devices, such as logic circuits, analog circuits, digital circuits, and mixed signal ICs are much more difficult to test as they are more complex and thus require more complex testing methodologies.

In general, for memory ICs, typically only bit swapping needs to be tested, and only the pattern may change from testing method to testing method (see, e.g., U.S. Patent No. 4,460,997 to Harns cited by the Examiner on the Examiner's PTO-892 Form). Occasionally with memory ICs the timing of the read-write cycle will need to be tested as well.

For logic circuits, special test procedures are required to make the logic work, such as procedures for switching power circuits of several amps within the IC, testing interfaces such as CAN, SPI, and RS232, and testing turn-on and turn-off temperatures.

For analog circuits, many tests are directed towards AC and DC gain, frequency response, frequency distortion, frequency analysis, amplitude, distortion and noise.

For digital circuits, typically the bit stream and the meaning of the bits in the bitstream needs to be analyzed.

Those skilled in the art will appreciate that Peters is limited to testing methods for memory ICs, and does not contemplate any testing methods that would typically be applicable to testing of logic circuits, analog circuits, digital circuits, or mixed-signal ICs.

Applicants' amended claim 1 is limited to mixed-signal ICs. A mixed-signal IC is defined as:

> *An integrated circuit that has both digital and analog functions on the same semiconductor chip, permitting a high degree of system integration.*

See attached web page from google.com resulting from search for "Define: mixed-signal IC."

In the passage relied on by the Examiner (Col. 2, lines 35-67), Peters discloses using AC

and DC testing parameters, but does not disclose or remotely suggest a mixed-signal IC which IC has both digital and analog functions on the same chip, as set forth in Applicants' amended claim 1.

In addition, Applicants respectfully submit that it is apparent from the Office Action that the Examiner has either misinterpreted Peters or Applicants' claim language. Each of Applicants' independent claims 1, 7, and 14 specifies "obtaining data and control instructions from multidimensional test matrices independent of a test environment, said multidimensional test matrices comprising one of matrix databases or libraries." The cited portion of Peters relied on by the Examiner (Col. 4, lines 19-40) refers to "memory array" and "array test specifications." Applicants respectfully submit that the term "array" as used in Peters is used to describe the memory array on the IC, and not the form of the test instructions being input by the operator. Therefore, the high level array test specifications 20 shown in Figure 2 must be interpreted as a high level test specifications for the memory arrays 25A, 25B, 25C, ..., 25X and not as an array itself (Col. 7, lines 58-62). In contrast to Peters, in Applicants' claimed invention, the multidimensional matrices such as matrix databases or libraries form the input from which the data and control instructions are obtained (see, e.g., Applicants' Figures 4 and 5).

Since Peters is limited to testing memory arrays, only a small variance of inputs are needed to complete the simple tests required. Therefore, Peters uses only menus on interactive data entry device 12 for the input, and not matrix databases or libraries as apparently assumed by the Examiner (See, Peters, Col. 4, lines 30-35).

Peters does not disclose or remotely suggest obtaining data and control instructions from multidimensional test matrices independent of a test environment, said multidimensional test matrices comprising one of matrix databases or libraries, as claimed by Applicants in claims 1, 7, and 14.

Further, in Peters, the universal language generator 14 is operated by presenting the user with an appropriate display screen in a predetermined sequence to facilitate the interactive entry of characterizing information (Col. 5, lines 34-41). In contrast, with Applicant's claimed invention according to independent claims 1, 7, and 14, the data and control instructions are

obtained from multidimensional test matrices, and not from sequentially provided display screens requiring user interaction.

Further, with Applicants' claimed invention, the data and control instructions are converted by means of a code generator into a syntax dependent on the test environment, and integrating the syntax dependent on the test environment into a general syntax dependent on the test environment to form the complete control. Peters is directly to the contrary. In Figure 1 of Peters relied on by the Examiner, the universal language generator 14 creates a universal, tester independent language instruction sequence 16. This tester independent language sequence 16 is then translated to specific tester sequences for each tester 30A, 30B, 30C, . . . 30X by individual universal to tester translators 19A, 19B, 19C . . .19X as assigned by universal to tester translator selector 18. Thus, Peters converts the input from menus into general tester independent language sequences which are then translated for a specific tester or testers. In contrast, with Applicants' claimed invention, input from a multidimensional test matrix provides data and control instructions which are independent of the test environment (without the need for a universal language generator) and the data and control instructions are converted directly into syntax which is dependent on the test environment. This syntax dependent on the test environment is then integrated into a general syntax dependent on the test environment.

Thus, the present invention does not employ a conversion of the input into a general language as required by Peters. Rather, with Applicants' claimed invention, the input data and control instructions obtained from the matrices are already in a test independent format. Further, while Peters does disclose converting test independent language sequences into test dependent sequences, Peters does not disclose integrating these test dependent sequences with general test dependent sequences to form a complete control.

Accordingly, Peters does not disclose or remotely suggest obtaining data and control instructions from a multidimensional matrix which data and control instructions are independent of the test environment, converting such data and control instructions by means of a code generator into a syntax which is dependent on the test environment and integrating the syntax dependent on the test environment into a general syntax dependent on the test environment, so

that the syntax dependent on the test environment and the general syntax dependent on the test environment together form a complete control, comprising analog and digital signals, for one of the specific test environments, as set forth in Applicants' claims 1, 7, and 14.

Applicants' claim 7 is analogous to claim 1 with the exception that it is not limited to mixed-signal ICs, and specifies that the individual specific test environments differ from one another in at least one of structure and syntax. Peters does not disclose or remotely suggest individual test environments that differ from one another in either structure or syntax, as set forth in Applicants' claim 7.

Applicants' claim 14 is analogous to claim 1 with the exception that it is not limited to mixed-signal ICs, and specifies that test methods which allow both digital and analog signals for the control of the test environment to occur synchronously are listed in the multidimensional test matrices. As discussed above, Peters does not disclose the use of a multidimensional test matrices as an input in generating the control. Accordingly, Peters cannot be interpreted to disclose or suggest that test methods which allow both digital and analog signals for the control of the test environment to occur synchronously are listed in the multidimensional test matrices, as set forth in Applicants' claim 14.

Similarly, Peters does not disclose or remotely suggest the features of Applicants' dependent claims.

As Peters does not disclose each and every element of the invention as claimed, the rejections under 35 U.S.C. § 102(b) are believed to be improper, and withdrawal of the rejections is respectfully requested. See, *Akamai Technologies Inc., supra.*

Applicants respectfully submit that the present invention is not anticipated by and would not have been obvious to one skilled in the art in view of Peters, taken alone or in combination with any of the other prior art of record.

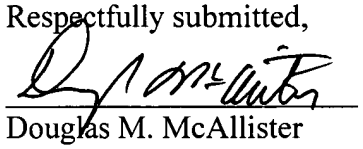
Further remarks regarding the asserted relationship between Applicants' claims and the prior art are not deemed necessary, in view of the foregoing discussion. Applicants' silence as to any of the Examiner's comments is not indicative of an acquiescence to the stated grounds of rejection.

Withdrawal of the rejections under 35 U.S.C. § 102(b) and 35 U.S.C. § 103(a) is therefore respectfully requested.

Conclusion

The Examiner is respectfully requested to reconsider this application, allow each of the pending claims and to pass this application on to an early issue. If there are any remaining issues that need to be addressed in order to place this application into condition for allowance, the Examiner is requested to telephone Applicants' undersigned attorney.

Respectfully submitted,



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